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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,488	02/22/2002	Henry Esmond Butterworth	GB919990129US1	8490

7590 04/13/2004

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,488	BUTTERWORTH ET AL.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

There are non-initialed alterations for the signature for William James Scales.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: there does not appear to be any support in the specification for the term "relative addresses".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

On page 17, lines 26-28, it is not clear where it is taught that the cached data is flushed prior to the temporarily suspending access. No order is indicated of flushing and suspending in lines 26-28.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schultz et al. (6,058,489) in view of Brady et al. (5,671,390).

As per claims 1, 12, 16, and 20, Schultz et al. teaches an information processing system including a host computer attached to a RAID-5 array of disk devices via a disk controller. See figures 1 and 2A and column 2, lines 41-43. An additional disk drive can be attached to an existing array of disk drives. See figure 2B and column 8, lines 37-38. As can be seen from figures 2B and 2C, an additional striping unit ("strip") is added to each row ("stripe") of the array of disks ("logically appending an additional strip...to the end of each stripe...").

Schultz et al. does not teach that the controller is a log structured array (LSA) controller which defines a directory of stripes. Brady et al. teaches the use of a log structured array storage subsystem comprised of a storage array and an array controller. See column 1, lines 46-49. The

LSA controller includes a directory which indicates the current physical location of data associated with each logical track on the disks of the array. See column 1, lines 26-30. It would have been obvious to one of ordinary skill in the art to have modified the controller of Schultz et al. to implement an LSA controller with a directory, as suggested by Brady et al., because Brady et al. teaches that an LSA storage subsystem provides an inexpensive, high performance, lower cost, and higher reliability system at column 1, lines 43-46.

Brady et al further teaches that each entry in the LSA directory includes a logical track number and a segment number X, segment column Ci, and a starting sector within a column Si, where X, Ci, and Si make up the physical address associated with the logical track. See column 7, lines 21-33, and column 8, lines 37-43. The values of X, Ci, and Si represents the claimed "relative address" (noting that Applicant states on page 16, lines 22-24, that the "segment column" of an LSA is the same as a RAID stripe and the block offset into a segment is the same as the block offset into the RAID stripe).

As per claims 2, 13, 15, and 21, Schultz et al. teaches that the array is a RAID-5 array as noted above, wherein a RAID-5 array is an N+1 array of N data locations and 1 parity location per stripe.

As per claims 3, 14, 18, and 22, the RAID-5 array of Schultz et al. includes stripes of N data striping units and 1 parity striping unit. As taught by Brady et al, each striping unit or segment of the array includes a plurality of logical tracks. See column 2, lines 43-45.

As per claim 4, 15, and 19, Brady et al. teaches that the directory indicates the current physical location of data associated with a logical track (see column 2, lines 30-31). Brady et al further teaches that each entry in the LSA directory includes a logical track number and a

segment number X, segment column Ci, and a starting sector within a column Si, where X, Ci, and Si make up the physical address associated with the logical track. See column 7, lines 21-33, and column 8, lines 37-43. The values of X, Ci, and Si represents the claimed "relative address" (noting that Applicant states on page 16, lines 22-24, that the "segment column" of an LSA is the same as a RAID stripe and the block offset into a segment is the same as the block offset into the RAID stripe).

As per claim 5, Schultz et al. and Brady et al. (see column 2, lines 8-15) teach a RAID-5 architecture, where the parity striping unit (segment-columns of Brady et al.) are rotated amongst the disk of the array. As shown by Shultz et al. in figure 2C, selected data (which can include parity strips) are moved to the newly added disk.

As per claim 6, Schultz et al. teaches that the disk array configuration is performed as a background task, i.e. during normal I/O operations to the storage devices. See the abstract.

As per claim 7, Schultz et al. teaches that the disk array configuration is performed as a background task by firmware on a disk controller board. See the abstract.

As per claim 8, Brady et al. teaches a bitmap at figures 5a-c, where the bitmap indicates which tracks are valid within a segment. See column 8, lines 47-67.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choy et al. (5,758,118) in view of Brady et al. (5,671,390).

As per claims 1, 12, 16, and 20, Choy et al. teaches an information processing system including a host 202 attached to a RAID-5 array of disk devices via a RAID master controller 204. See figure 2 and column 5, lines 14-15. An additional disk drive 222 can be attached to an existing array of disk drives. See column 5, lines 30-31. As can be seen from figure 4, an

additional "strip" (column 406 of table 400) is added to each row ("stripe") of the array of disks ("logically appending an additional strip...to the end of each stripe...").

Choy et al. does not teach that the controller is a log structured array (LSA) controller which defines a directory of stripes. Brady et al. teaches the use of a log structured array storage subsystem comprised of a storage array and an array controller. See column 1, lines 46-49. The LSA controller includes a directory which indicates the current physical location of data associated with each logical track on the disks of the array. See column 1, lines 26-30. It would have been obvious to one of ordinary skill in the art to have modified the controller of Choy et al. to implement an LSA controller with a directory, as suggested by Brady et al., because Brady et al. teaches that an LSA storage subsystem provides an inexpensive, high performance, lower cost, and higher reliability system at column 1, lines 43-46.

Brady et al further teaches that each entry in the LSA directory includes a logical track number and a segment number X, segment column Ci, and a starting sector within a column Si, where X, Ci, and Si make up the physical address associated with the logical track. See column 7, lines 21-33, and column 8, lines 37-43. The values of X, Ci, and Si represents the claimed "relative address" (noting that Applicant states on page 16, lines 22-24, that the "segment column" of an LSA is the same as a RAID stripe and the block offset into a segment is the same as the block offset into the RAID stripe).

As per claims 2, 13, 15, and 21, Choy et al. teaches that the array is a RAID-5 array as noted above, wherein a RAID-5 array is an N+1 array of N data locations and 1 parity location per stripe.

As per claims 3, 14, 18, and 22, the RAID-5 array of Choy et al. includes stripes of N data striping units and 1 parity striping unit. As taught by Brady et al, each striping unit or segment of the array includes a plurality of logical tracks. See column 2, lines 43-45.

As per claim 4, 15, and 19, Brady et al. teaches that the directory indicates the current physical location of data associated with a logical track (see column 2, lines 30-31). Brady et al further teaches that each entry in the LSA directory includes a logical track number and a segment number X, segment column Ci, and a starting sector within a column Si, where X, Ci, and Si make up the physical address associated with the logical track. See column 7, lines 21-33, and column 8, lines 37-43. The values of X, Ci, and Si represents the claimed "relative address" (noting that Applicant states on page 16, lines 22-24, that the "segment column" of an LSA is the same as a RAID stripe and the block offset into a segment is the same as the block offset into the RAID stripe).

As per claim 5, Choy et al. and Brady et al. (see column 2, lines 8-15) teach a RAID-5 architecture, where the parity striping unit (segment-columns of Brady et al.) are rotated amongst the disk of the array. As shown by Choy et al. in figure 4, selected data (which can include parity strips) are moved to the newly added disk.

As per claims 6 and 7, Choy et al. teaches that the disk array configuration is performed by the controller, i.e. during normal I/O operations to the storage devices, and is therefore a background task to the host device. See column 5, lines 3-5.

As per claim 8, Brady et al. teaches a bitmap at figures 5a-c, where the bitmap indicates which tracks are valid within a segment. See column 8, lines 47-67.

As per claim 9, Choy et al. teaches initializing the newly added disk to all binary zeros at column 5, lines 27-30.

As per claim 10, Choy et al. teaches adding one or more ("plurality of...") DASDs to the RAID array at column 3, lines 5-7.

As per claim 11, Choy et al. teaches adding a new disk to a RAID-5 disk array. See column 4, lines 54-55. With reference to figure 6, a new DASD is initialized in step 604, which involves pre-storing binary zeros to the new DASD ("initializing the new disk..."). See column 9, lines 38-41. The controller suspends operations ("temporarily suspending access"; step 607 and column 9, lines 42-44) and writes out to DASD modified parity tracks in the cache/invalidates parity tracks in the cache ("flushing any data cached"; step 609 and column 9, lines 45-47). The new DASD is brought on-line ("adding the new disk"; step 608) and parity data is relocated ("applying an algorithm to relocate the parity"; step 610 and column 9, lines 55-59).

Response to Arguments

8. Applicant's arguments filed 05 March 2004 have been fully considered but they are not persuasive.

Applicant argues that Brady et al. does not teach "relative addressing", however Brady et al. teaches "relative addressing" as set forth above in the rejection of the claims under 35 USC 103(a).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
April 12, 2004